8.1 (Reserved)

8.2 ATTACHED PAYLOADS

8.2.1 Payload Data Interleaver (PDI) Interface

The Orbiter shall provide for the acquisition of asynchronous Payload Pulse Code Modulation (PCM) telemetry data via the PDI. Refer to Figure 8.2.1-1 for PDI data flow.

8.2.1.1 PDI Input Data Characteristics-Shuttle Standard Formats

Refer to Section 20 paragraph, 20.4

Note: A non-compliance condition exists between the Orbiter and the MIGHTY. Refer to Section 20 for the definition of the unique interface requirement.

The Shuttle Orbiter Standard Telemetry Formats for Payloads are three in number, and are designated Format Synchronization Mode Type 1 Format, Type 2 Format, and Type 3 Format. The distinctive characteristic of these three types of Payload PCM Telemetry formats is that their structure enables both the Orbiter's PDI and the Orbiter's GPC software services to process Payload measurement data, and as a group satisfies the requirements of Table 8.2.1.1-1 and Figure 8.2.1.1-1, Figure 8.2.1.1-2, and the figures associated with the three formats defined in the subparagraphs. Each of these three Shuttle Standard Formats also enables the PDI to process Payload Frame data as Time Homogenous Data Sets for inclusion within the Orbiter's PCM Telemetry Downlink.

With respect to the Orbiter's PCM Telemetry Downlink, a Time Homogenous Data Set (THDS) is defined to be those eight bit words decommutated from a Payload frame such that those words from one Payload frame shall never be mixed with those words from any other Payload frame within either the PDI or PCMMU (PCM Master Unit) (refer to Figure 8.2.1.1-3). With respect to Orbiter GPC software services, maintaining the time homogeneity for both individual multiword Payload measurements and Payload measurement word sets cannot be guaranteed.

8.2.1.1.1 Type 1 Format NOT APPLICABLE

8.2.1.1.2 Type 2 Format NOT APPLICABLE

8.2.1.1.3 Type 3 Format

A Type 3 Payload Format is herein defined as a format consisting of Master Frames and Minor Frames as shown in Figure 8.2.1.1.3-1. Every Minor Frame shall be identified by a Minor Frame Sync pattern which occurs once each Minor Frame, and shall be the same sync pattern for all Minor Frames.

A Master Frame, in general, shall contain two or more Minor Frames; otherwise, there is no distinction with a Type 1 Format. Additionally, every Minor Frame shall contain an eight bit Minor Frame Count word. The start of a Master Frame shall be identified as the Minor Frame which contains an initial value of the Minor Frame Count word.

8.2.1.1.3.1 Orbiter PCM TLM Downlink Service

Throughputting Payload data to the ground via the Orbiter's PCM TLM Downlink is implemented via the PDI's Toggle Buffer for individual Minor Frames. Before individual Minor Frames can be transferred to the PDI's Toggle Buffer, recognition by the PDI of two successive valid Minor Frame Sync patterns must first occur. When this has happened, Toggle Buffer storage for each Minor Frame shall proceed as follows:

a. The THDS within the PDI's Toggle Buffer shall, in part, consist of a complete Minor Frame or a subset thereof. The subset may consist of any number of uniquely identifiable contiguous or noncontiguous 8-bit Minor Frame words. The THDS to be downlinked shall be an even number of 8-bit words. If an even number of 8-bit words are not specified, the PDI will add 8-bits of fill data.

b. The remainder of the THDS shall consist of three additional 16 bit Status Words appended to the Minor Frame words by the PDI as shown in Figure 8.2.1.1-3.

8.2.1.1.3.2 Orbiter GPC Software Service NOT APPLICABLE

8.2.1.2 PDI Input Data Characteristics-Shuttle Non Standard Formats NOT APPLICABLE

8.2.1.3 Electrical Interface Characteristics

For Payloads using one of the three Biϕ data codes (Biϕ-L, M or S), the PDI is capable of extracting associated Clock information and determining bit period boundary definition.

For Payloads using one of the three NRZ data codes (NRZ-L, M or S), the PDI requires the Payload to provide a CLOCK interface along with the DATA interface so as to enable the PDI to determine bit period boundary definition.

8.2.1.3.1 PDI Data Input

The PDI Data input electrical interface characteristics at the Orbiter/payload interface shall be as defined in Table 8.2.1.3.1-1 and Figures 8.2.1.3.1-1, 8.2.1.3.1-2 and 8.2.1.3.1-3.

8.2.1.3.2 PDI Clock Input NOT APPLICABLE

8.2.1.4 (Reserved)

8.2.1.5 Grounding and Shielding

Grounding and shielding shall be as shown in Figure 8.2.1.5-1.

8.2.2 Multiplexer/Demultiplexer (MDM) Interface NOT APPLICABLE

8.2.3 Orbiter/Payload Recorder (OPR) Interface NOT APPLICABLE

TABLE 8.2.1.1-1 PDI INPUT DATA CHARACTERISTICS-ATTACHED INTERFACE SHUTTLE STANDARD FORMAT

Parameter	Dimension	PDI Tolerance	Data Formats 1	2	3	Notes
Bit rate (center frequency)	bps	10 bps to 8 kbps	x	x	x	(1)
Input Signal Code		NRZ-L NRZ-M NRZ-S Biϕ-L Biϕ-M Biϕ-S	x	x	x	(2)
Word length	Bits	8 or multiples of 8	x	x	x	(3)
Master Frame Length	Words	8 to 1024 (8-bit words)	x			(4)
	or					
	Minor Frames	2 to 256		x	x	(5)
Master Frame Sync	Bits	8, 16, 24 or 32	x			(6)
	Bits	8 bits of unique sync pattern		x		(7)
	Bits	8 bit Minor Frame Counter			x	(8)
Minor Frame Length	Words	8 to 1024 (8-bit words)		x	x	
Minor Frame Sync	Bits	8, 16, 24, or 32		x	x	(9)
Frame Rate	Master Frame/Sec	200 maximum	x			
	Minor Frames Per Sec	200 maximum		x	x	
Formats Sample Rates (Non-standard)	Samples/Master Frame	Limited only by payload input bit rate	x	x	x	(10)

Table 8.2.1.1-1 PDI INPUT DATA CHARACTERISTICS-ATTACHED INTERFACE SHUTTLE STANDARD FORMAT (CONTINUED)

Parameter	Dimension	PDI Tolerance	Data Formats 1	2	3	Notes
Format Sample Rates (Standard)	Samples/Master Frame	Master Frame rate only	x			(11)
		One equal to Minor Frame rate		x	x	(12)(13)
		Six equal to integer submultiple of Minor Frame rate.		x		(12)(13)

Notes:

(1) A maximum of up to 8kbps is allocated for small payload usage.

(2) Refer to Figure 8.2.1.1-1. Bit rate clock is required with NRZ codes.

(3) Bit pattern for the data word in the incoming data stream from the payload in terms of Most Significant Bit (MSB) through Least Significant Bit (LSB), with the following examples, shall be defined by the payload.

(4) Refer to Figure 8.2.1.1.1-1.

(5) Refer to Figures 8.2.1.1.2-1 and 8.2.1.1.3-1.

(6) Any pattern (with exception FAF320 hexadecimal bit pattern shall not be used) of contiguous bit position located in first or last word(s) of every master frame. Utilization of the last word(s) may preclude telemetry data stream processing at KSC.

(7) Any pattern located within the first or last minor frame in any word column, other than the minor frame sync word column(s).

Table 8.2.1.1-1 PDI INPUT DATA CHARACTERISTICS-ATTACHED INTERFACE SHUTTLE STANDARD FORMAT (CONCLUDED)

(8) Ascending or descending binary count which increments or decrements one count each minor frame. Initial count value is programmable. Count pattern shall always be Most Significant Bit (MSB) first and right justified. Location of the minor frame count word within each minor frame can be any word column, other than minor frame Sync word column(s), but has to be the same for every minor frame.

An example of the Minor Frame Counter (MFC) with a Type 3 format with 8 minor frames is as follows:

The initial value of the MFC is 00000000, signifying the start of the master frame. The MFC increments each minor frame to a count of 00000111, signifying end of master frame.

(9) Any pattern of contiguous bit positions located in first or last word(s) of every minor frame. (See Note 6 for KSC limitations.)

(10) For those payloads which require no Orbiter GPC software services (payload data via the PDI toggle buffer only), their PCM telemetry formats can utilize nonstandard sample rates. Any sample rate which is not an integer multiple/submultiple of the payload frame rate is considered a nonstandard rate.

(11) Refer to Figure 8.2.1.1-2. Payloads measurements within the Master Frame (Type 1) whose measurements are at the Master Frame rate can be processed by the PDI only when multiple Measurement Stimulus Identification (MSID) numbers are used to specify each payload measurement.

(12) Format Types 2 or 3 shall contain a maximum of seven sample rates per format. One of the sample rates shall be equal to the number of minor frames per master frame. The remaining six sample rates shall be any submultiple of the minor frame rate as described by Figure 8.2.1.1-2.

(13) Refer to Figure 8.2.1.1-2. Payload measurements within the minor frame whose sample rates are integer multiples of the minor frame rate can be processed by the PDI but only when multiple MSID numbers are used to specify each payload measurement.

Each payload measurement is identified by a unique alphanumeric code (MSID) assigned by NASA/JSC as directed by "Space Shuttle Master Measurement List", document number JSC-08220.

The PDI is not capable of processing payload sample rates which are less than the smallest integer submultiple of the payload minor frame rate (Y) as defined within Figure 8.2.1.1-2.

TABLE 8.2.1.3.1-1 PDI DATA INPUT/PAYLOAD-TO-ORBITER ELECTRICAL INTERFACE CHARACTERISTICS

Parameter	Dimension	Characteristics Orbiter/Payload Interface	Notes
Signal Type		Differential-Balanced	Refer to Figures 8.2.1.3.1-1 and 8.2.1.3.1-2
Amplitude	Volts pk-pk	2.6 Min 9.0 Max	Measured line-to-line
Duty Cycle	Percent	50 ± 5	(1)(2)
Bit-Rate Accuracy	Percent	±3.25	(3)
Stability		≤ 1 part in 10^5 over 60 sec Period	
Waveform Distortion		Overshoot and undershoot less than 20 percent of peak amplitude level	
Noise	Milli-volts	50 pk-pk, differential line-to-line, DC to 100 kHz	Payload transmitting, not transmitting, or failed
Cable		2 conductor twisted, shielded, jacketed, controlled impedance	Rockwell design standard MP572-0328-0002
Cable impedance Zo	Ohm	70 Min 80 Max	Measured conductor to conductor at 1 MHz
Cable Capacitance (Orbiter)	Pico-farads	3749 Max	(8)
Input Impedance (Orbiter)	Ohm	70 Min 94 Max	DC resistance line-to-line includes cable resistance (8)
Rise/Fall Time		Max: Refer to Differential Phase Skew	(4) RT/FT are independent of bit rate and data code type (Biϕ or NRZ).

TABLE 8.2.1.3.1-1 PDI DATA INPUT/PAYLOAD-TO-ORBITER ELECTRICAL INTERFACE CHARACTERISTICS (Continued)

Parameter	Dimension	Characteristics Orbiter/Payload Interface	Notes
Skew-Differential Phase	Nano-second to Milli-second depending on payload bit rate		(5) (7)
For Biϕ data:		Max: $Tp - .841Tp - (1x10^{-6}) - 2NTp - .125x10^{-6} -$ $T_{LR}\left[LOG_e\left(\frac{V_{LPK} - 100\text{ millivolts}}{V_{LPK} - 300\text{ millivolts}}\right)\right] -$ $T_{TR}\left[LOG_e\left(\frac{V_{TPK} + 300\text{ millivolts}}{V_{TPK} + 100\text{ millivolts}}\right)\right]$ Where: N = Payload Duty Cycle Offset $0 \le N \le 0.05$ V_{LPK} = Peak amplitude level of Biϕ waveform leading edge. V_{TPK} = Peak amplitude level of Biϕ waveform trailing edge. Tp = Reciprocal of max. payload bit rate. T_{LR} = Max. rise time of Biϕ waveform leading edge measured between 10 percent and 90 percent points. T_{TR} = Max. fall time of Biϕ waveform trailing edge measured between 10 percent and 90 percent points.	

TABLE 8.2.1.3.1-1 PDI DATA INPUT/PAYLOAD-TO-ORBITER ELECTRICAL INTERFACE CHARACTERISTICS (Continued)

Parameter	Dimension	Characteristics Orbiter/Payload Interface	Notes
Skew-Differential Phase (Cont.)			
For NRZ data:		Max: Tp - .691Tp - NTp - $T_{CR}\left[\log_e\left(\frac{V_{CPK} - 100\text{ millivolts}}{V_{CPK} - 300\text{ millivolts}}\right)\right]$ - $T_{DR}\left[\log_e\left(\frac{V_{DPK} + 300\text{ millivolts}}{V_{DPK} + 100\text{ millivolts}}\right)\right]$ Where: N = Payload Clock Duty Cycle Offset $0 \le N \le 0.05$ V_{CPK} = Peak amplitude level of Payload CLOCK signal. V_{DPK} = Peak amplitude level of Payload NRZ DATA signal Tp = Reciprocal of max. payload bit rate (Center Frequency) T_{CR} = Max. transition time (rise or fall time) of payload CLOCK signal measured between 10 percent and 90 percent points. T_{DR} = Maximum transition time (rise or fall time) of payload NRZ DATA signal measured between 10 percent and 90 percent points.	

TABLE 8.2.1.3.1-1 PDI DATA INPUT/PAYLOAD-TO-ORBITER ELECTRICAL INTERFACE CHARACTERISTICS (Continued)

Parameter	Dimension	Characteristics Orbiter/Payload Interface	Notes
Common Mode	Volt	Not to exceed ±3, Line to ground	(6) Payload and PDI Connected

(1) Relative position of Biϕ-L mid bit transition at interface.

(2) Any bit or clock transition point occurs in time at the 50 percent pk-pk amplitude point.

(3) The PDI shall set an error flag within its BITE Status Register whenever the Payload bit rate exceeds ±3.25 percent of its specified center frequency.

(4) The maximum limit for Payload signal Rise/Fall time is not to be determined independently, but instead is to be determined as part of a tradeoff with other related offsets. In order to make that tradeoff, the appropriate general case equation for Differential Phase Skew shall be utilized.

(5) These two general case equations for Biϕ data and NRZ data are an expression of how the Payload bit period is partitioned between the PDI’s Bit Lock Range, Payload Duty Cycle Offset, PDI Programmed Bit Rate Offset (for Biϕ data only), and Payload maximum Rise and Fall time. The solution for each of these two general case equations indicates that amount of the Payload bit period which remains for partitioning between the payload signal Differential Phase Skew and/or Phase Shift. A solution for either of these two general case equations which produces a negative result indicates that the appropriate Offsets themselves have utilized all the remaining Payload bit period such that none is available for Differential Phase Skew and/or Phase Shift. PDI Bit Lock Range identifies the absolute minimum amount of the Payload bit period required for the PDI’s Bit Synchronizer to achieve and maintain bit lock.

Data Type	Bit Lock Range
Biϕ	$0.841Tp + (1x10^{-6})$
NRZ	0.691Tp

Payload Signal Differential Phase Skew, as defined here, shall consist of the absolute value of the difference between the Leading Edge Phase Shift and the Trailing Edge Phase Shift (refer to Figure 8.2.1.3.1-3), and is independent of Payload amplitude level.

TABLE 8.2.1.3.1-1 PDI DATA INPUT/PAYLOAD-TO-ORBITER
ELECTRICAL INTERFACE CHARACTERISTICS (Continued)

Payload Signal Phase Shift is the time differential between the 50 percent points of associated amplitude transitions of the two Payload differential inputs.

PDI Programmed Bit Rate Offset shall be 0.125 μsec for all Biϕ data rates from 10 bps to 64 kbps.

(6) Volts over frequency spectrum from DC to 100 KHZ.

(7) The example illustrates how the Biϕ Data general case equation for Differential Phase Skew shall be utilized by a Payload user. The following Payload interface characteristics are utilized as part of the first tradeoff for determining the Payload user's upper limit for each of the Offsets applicable to that Payload.

Bit Rate (Center Frequency):	1600 BPS
Biϕ Data Duty Cycle:	50 ± 5 percent
Biϕ Data Peak Amplitude:	1.25 volts
Maximum Transition Time: (Rise and Fall Time)	5 μsec

For the specified center frequency of 1600 BPS, the corresponding amount of time for one bit period is:

$$Tp = \frac{1}{1600\ BPS} = 625\ \mu seconds.$$

Within each Payload bit period (Tp), the general case equation for Biϕ Data Differential Phase Skew provides for the following amounts to Tp time to be dedicated to:

a) PDI's Bit Lock Range:

$$0.841Tp + (1x10^{-6}) = 0.841(625\ \mu sec) + 1\ \mu sec = 526.625\ \mu sec$$

b) Payload Biϕ Data Duty Cycle Offset: O.125μsec

$2NTp = 2(0.05)(625\ \mu sec) = 62.50\ \mu sec$ with
N = 0.05 corresponding to a 5 percent Duty Cycle Shift.

c) PDI Programmed Bit Rate Offset: 0.125 μsec

d) Ambiguity in Change of PDI Receiver Output Due to Slow Transition Time of Payload Data Differential Inputs:

$$T_{LR}\left[LOG_e\left(\frac{V_{LPK} - 100\ MV}{V_{LPK} - 300\ MV}\right)\right] + T_{TR}\left[LOG_e\left(\frac{V_{TPK} + 300\ MV}{V_{TPK} + 100\ MV}\right)\right] =$$

TABLE 8.2.1.3.1-1 PDI DATA INPUT/PAYLOAD-TO-ORBITER ELECTRICAL INTERFACE CHARACTERISTICS (Concluded)

$$5\mu sec \left[LOG_e \left(\frac{1.25 - 0.10}{1.25 - 0.30} \right) \right] + 5\mu sec \left[LOG_e \left(\frac{1.25 + 0.30}{1.25 + 0.10} \right) \right] =$$

$$5\mu sec \left[LOG_e \ (1.21) \right] + 5\mu sec \left[LOG_e \ (1.15) \right] = 1.64\mu sec$$

The remaining amount of TP time which is available to the Payload user for partitioning between Payload Biϕ Data Differential Phase Skew and/or Phase Shift is:

Diff. Phase Skew/Phase Shift =
$625\mu sec - 526.625\mu sec - 62.5\mu sec - 0.125\mu sec - 1.64\mu sec = 34.11\mu sec$.

This completes the first tradeoff such that the general case equation for Biϕ Data Differential Phase Skew has enabled the Payload user to dedicate the following amounts of time as upper limits for:

$0 \leq$ Duty Cycle Offset $\leq 62.5\ \mu$seconds

$0 \leq$ Transition Time Ambiguity $\leq 1.64\ \mu$seconds

$0 \leq$ Diff. Phase Skew/Phase Shift $\leq 34.11\ \mu$seconds

If these upper limits are acceptable, then the Payload user shall determine the actual amounts of time to be allocated to each appropriate Offset. If these upper limits are not acceptable, then the Payload user shall have to develop a <u>second tradeoff</u> with an appropriate change in either the Duty Cycle Shift, Maximum Transition Time, or Peak Amplitude. It should be noted that a Payload user can only change PDI Bit Lock Range by choosing a different Payload Bit Rate.

The general case equation for NRZ Data Differential Phase Skew is utilized in a manner identical to its Biϕ Data counterpart with the exception that PDI Programmed Bit Rate Offset is not included.

(8) Calculations based upon 163 feet from PDI to payload interface (end of 30 ft SPAT extender cable).

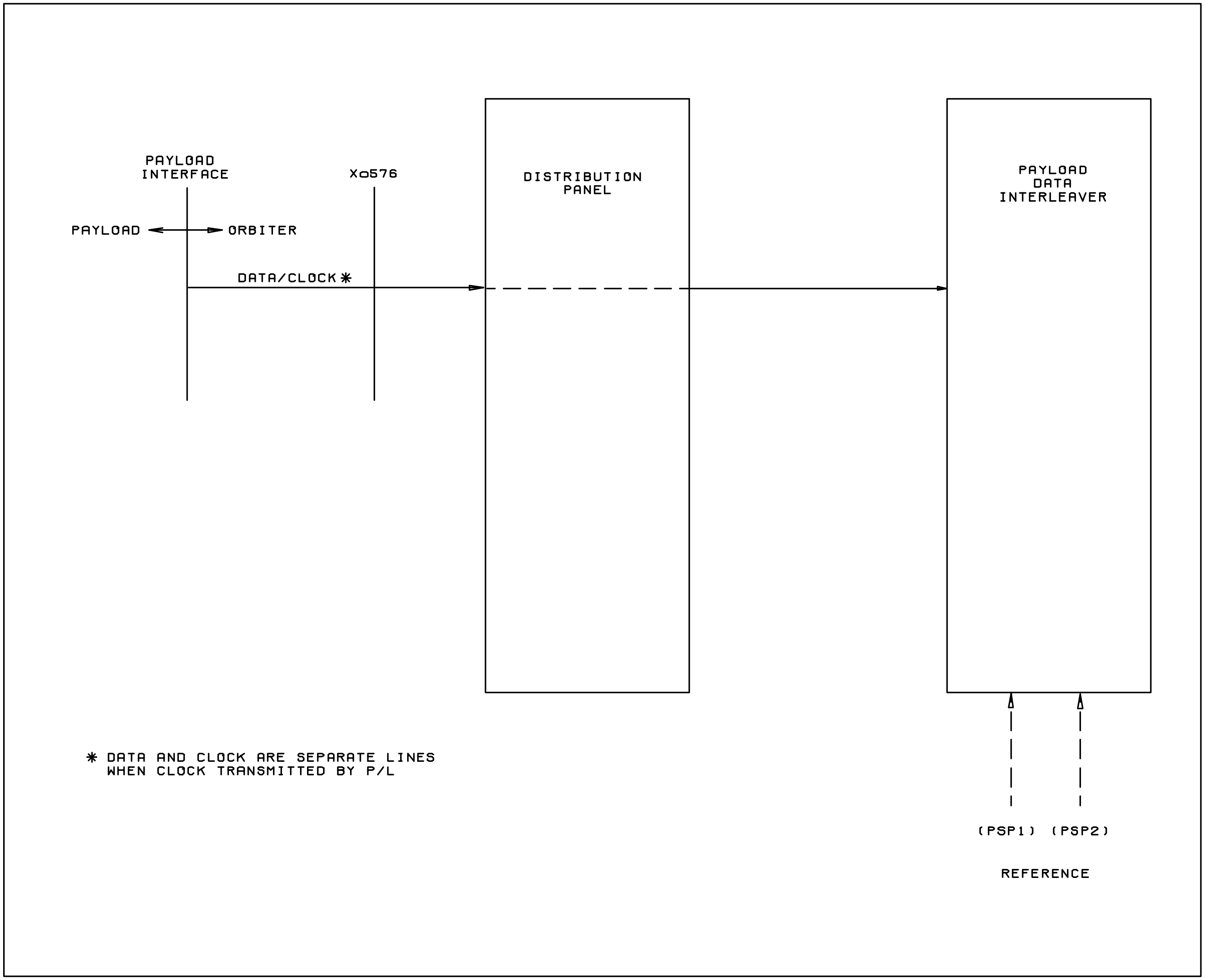
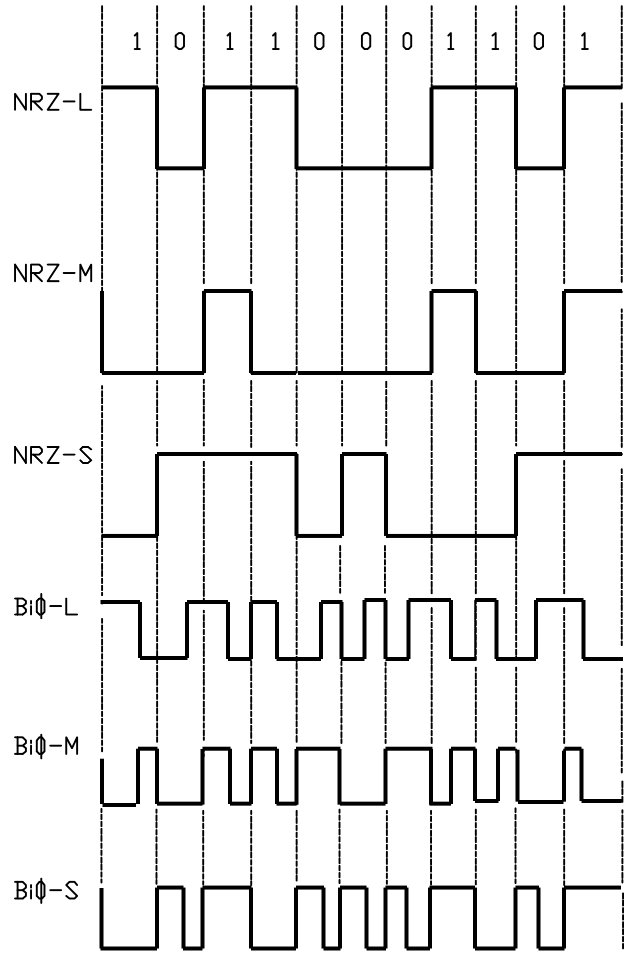


FIGURE 8.2.1-1 PAYLOAD DATA INTERLEAVER DATA FLOW



NRZ-LEVEL (OR NRZ CHANGE):
"ONE" IS REPRESENTED BY ONE LEVEL;
"ZERO" IS REPRESENTED BY THE OTHER LEVEL

NRZ-MARK
"ONE" IS REPRESENTED BY A CHANGE IN LEVEL;
"ZERO" IS REPRESENTED BY NO CHANGE IN LEVEL

NRZ-SPACE
"ONE" IS REPRESENTED BY NO CHANGE IN LEVEL:
"ZERO" IS REPRESENTED BY A CHANGE IN LEVEL

BI-PHASE LEVEL (OR BI-PHASE-CHANGE):
A TRANSITION OCCURS AT CENTER OF EVERY BIT PERIOD;
"ONE" IS REPRESENTED BY A "ONE" LEVEL WITH THE TRANSITION TO THE "ZERO" LEVEL.
"ZERO" IS REPRESENTED BY A "ZERO" LEVEL WITH THE TRANSITION TO THE ONE LEVEL

BI-PHASE-MARK:
A TRANSITION OCCURS AT THE BEGINNING OF EVERY BIT PERIOD;
"ONE" IS REPRESENTED BY A MIDBIT TRANSITION;
"ZERO" IS REPRESENTED BY NO MIDBIT TRANSITION

BI-PHASE SPACE:
A TRANSITION OCCURS AT THE BEGINNING OF EVERY BIT PERIOD;
"ONE" IS REPRESENTED BY NO MIDBIT TRANSITION;
"ZERO" IS REPRESENTED BY A MIDBIT TRANSITION

FIGURE 8.2.1.1-1 PCM INPUT CODES

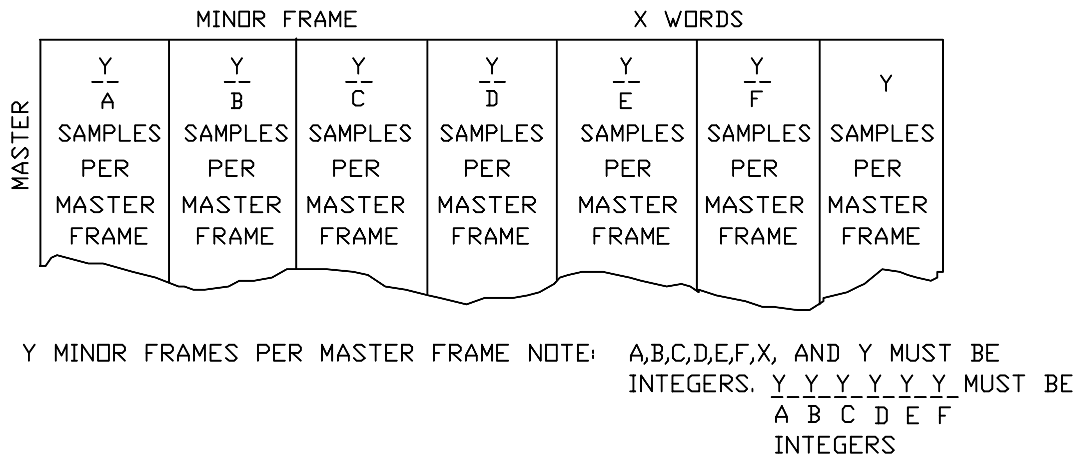
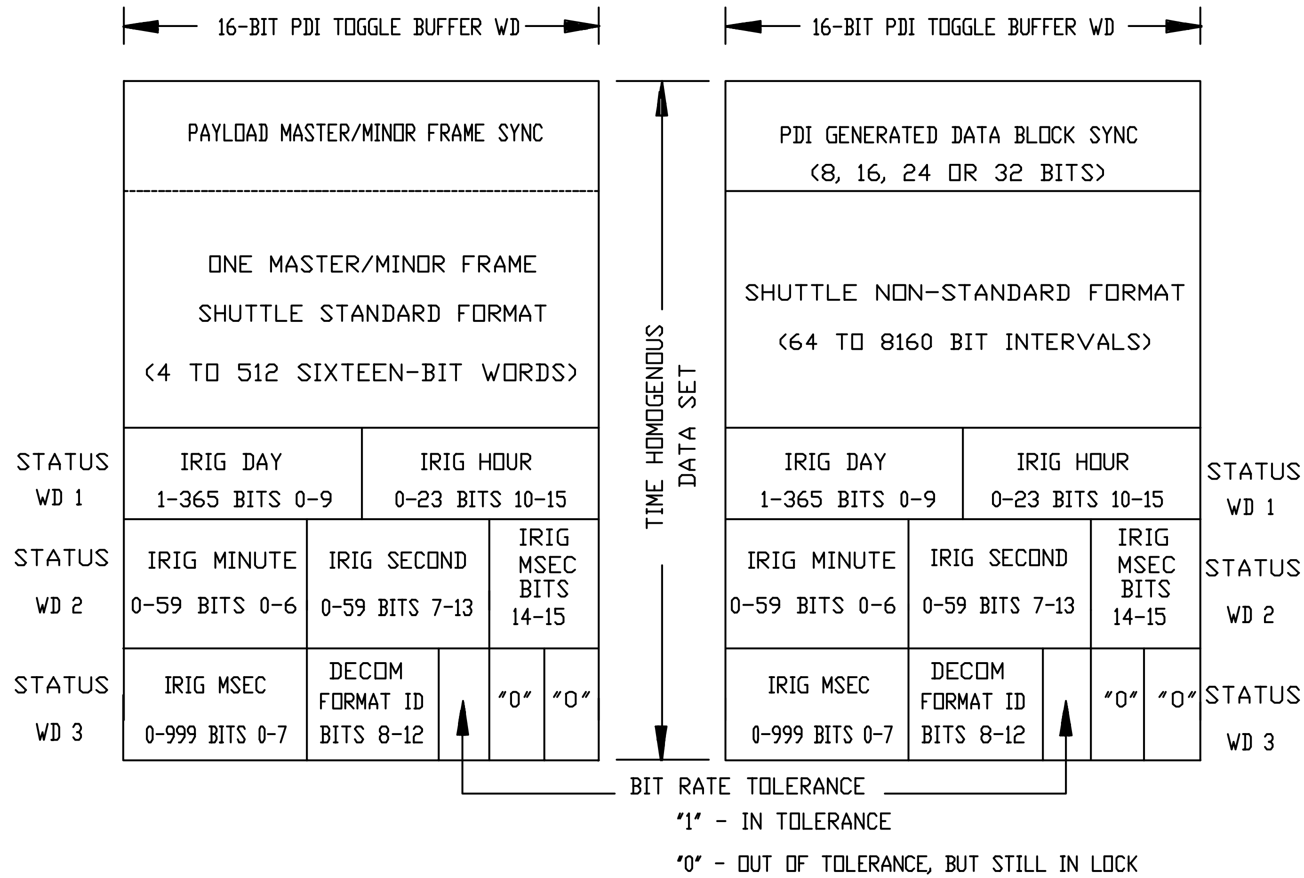


FIGURE 8.2.1.1-2 SHUTTLE STANDARD FORMAT SAMPLE RATES



IRIG DAY, HOUR, MINUTE, AND SECOND ARE BCD CODED, MSB FIRST

IRIG MSEC IS BINARY CODED, MSB FIRST

FIGURE 8.2.1.1-3 FRAME DATA SET STATUS WORDS

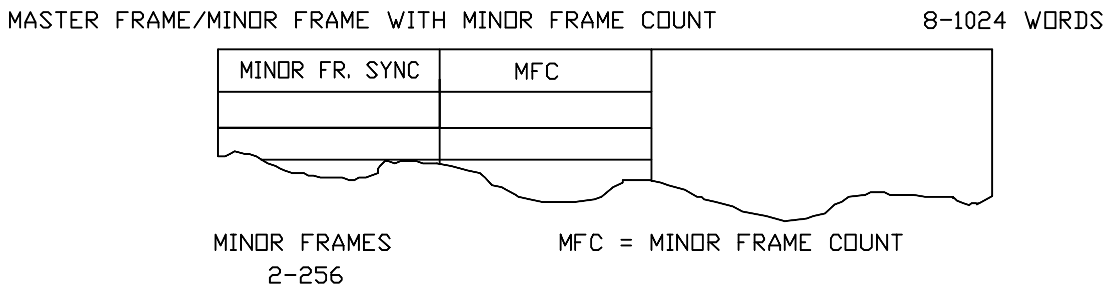
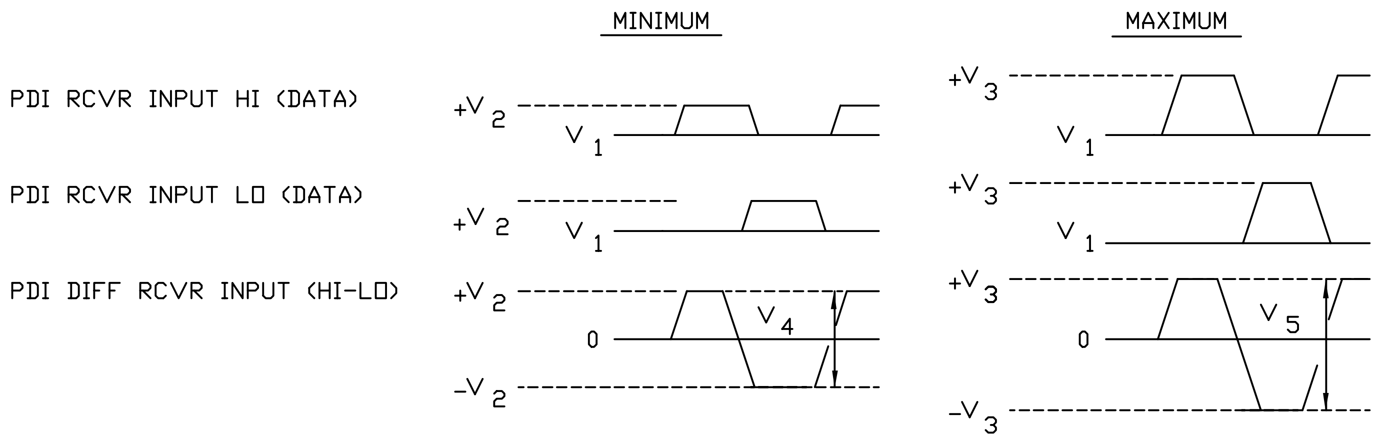


FIGURE 8.2.1.1.3-1 TYPE 3 SHUTTLE STANDARD FORMAT

FIGURE 8.2.1.3.1-1 DATA/DATA (INVERSE) - DIFFERENTIAL TRANSMISSION



V_1 = SIGNAL GROUND

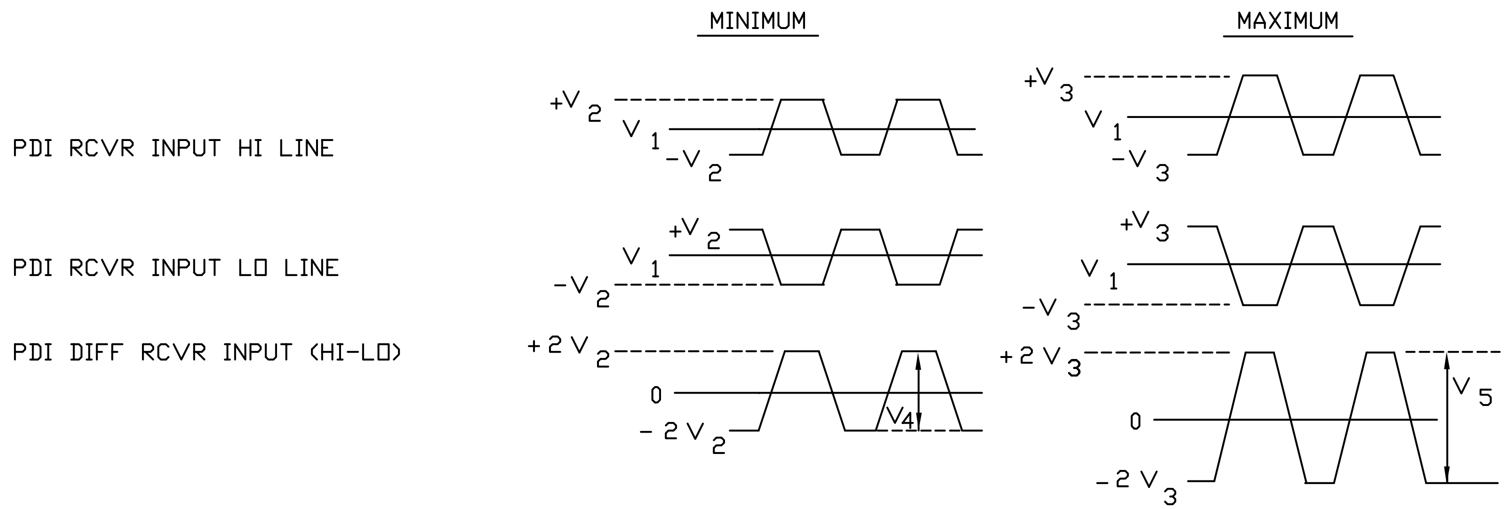
V_2 = 1.25 VOLTS LINE TO SIG. GND

V_3 = 4.5 VOLTS LINE TO SIG. GND

V_4 = 2.5 VOLTS P-P LINE-TO-LINE DIFFERENTIAL BALANCED

V_5 = 9.0 VOLTS P-P LINE-TO-LINE DIFFERENTIAL BALANCED

FIGURE 8.2.1.3.1-2 BI-POLAR LINES - DIFFERENTIAL TRANSMISSIONS



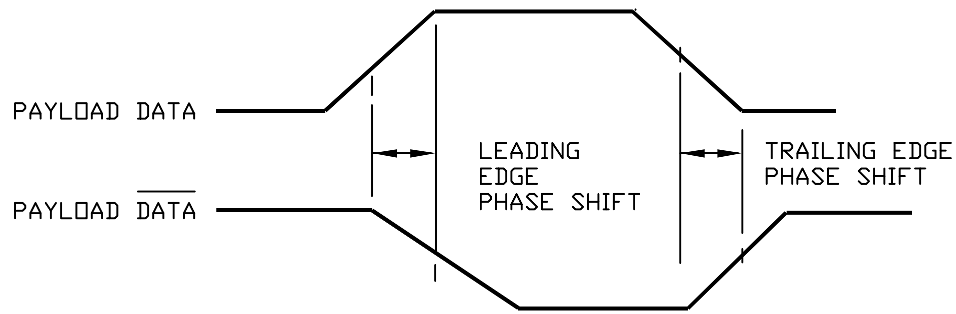
V_1 = SIGNAL GROUND

V_2 = 0.625 VOLTS LINE TO SIG. GND

V_3 = 2.25 VOLTS LINE TO SIG. GND

V_4 = 2.5 VOLTS P-P DIFFERENTIAL LINE-TO-LINE BALANCED

V_5 = 9.0 VOLTS P-P DIFFERENTIAL LINE-TO-LINE BALANCED



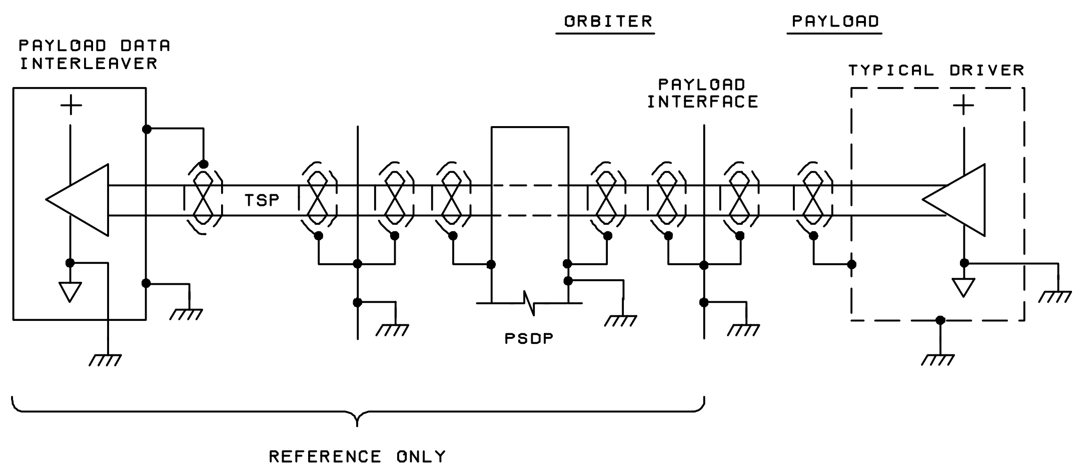
DIFFERENTIAL PHASE SKEW = LEADING EDGE PHASE SHIFT - TRAILING EDGE PHASE SHIFT

WHERE:

LEADING/TRAILING EDGE PHASE SHIFT IS THE TIME DIFFERENTIAL BETWEEN 50% POINTS OF ASSOCIATED AMPLITUDE TRANSITIONS OF THE DIFFERENTIAL INPUTS

FIGURE 8.2.1.3.1-3 DIFFERENTIAL PHASE SKEW

FIGURE 8.2.1.5-1 PAYLOAD DATA INTERLEAVER GROUNDING AND SHIELDING INTERFACE

PARAGRAPH	GROUNDING AND SHIELDING TERMINATIONS
8.2.1.3.1 PDI DATA INPUT 8.2.1.3.2 PDI CLOCK INPUT	 NOTE: CIRCUIT REFERENCE SYMBOLS DEFINED IN SECTION 10.7.4.2.4

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