UNIVERSITY OF ARIZONA
STUDENT SATELLITE PROJECT

Technical Note

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Revision 1.0: Initial Draft

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1. Document Overview

This document will provide details on overall design, structure and organization of DCH Flight Hardware.

2. Requirements

2.1 All DCH hardware must withstand radiation of minimum 5Krads

2.2 The hardware must automatically detect and attempt to correct all internal errors

The Flight Hardware will have Error Detection and Error Correction circuitry, which will detect and attempt to correct soft and hard errors. If an unrecoverable error is encountered, the system will be reset to the initial state.

2.3 DCH Hardware has to provide centralized control for all other satellite systems

DCH Hardware will monitor the status of other satellite systems, turn power on/off, read sensors information and perform other housekeeping activities.

3. Descriptions/Designs/Discussion

3.1 Processor

The DCH Flight Hardware will be based on Intel386™EX Embedded Processor. Before we chose this processor, we considered several other processors from Embedded Intel386™ Family (for side-to-side comparisons of the Embedded Intel386™ Family processors see Table 4-1 through Table 4-5). We have chosen this processor mainly because of its low power consumption and suitable peripheral

options. In addition, this processor has big enough range of operating temperatures (from –40 °C to +118 °C) which does not depend on packaging.

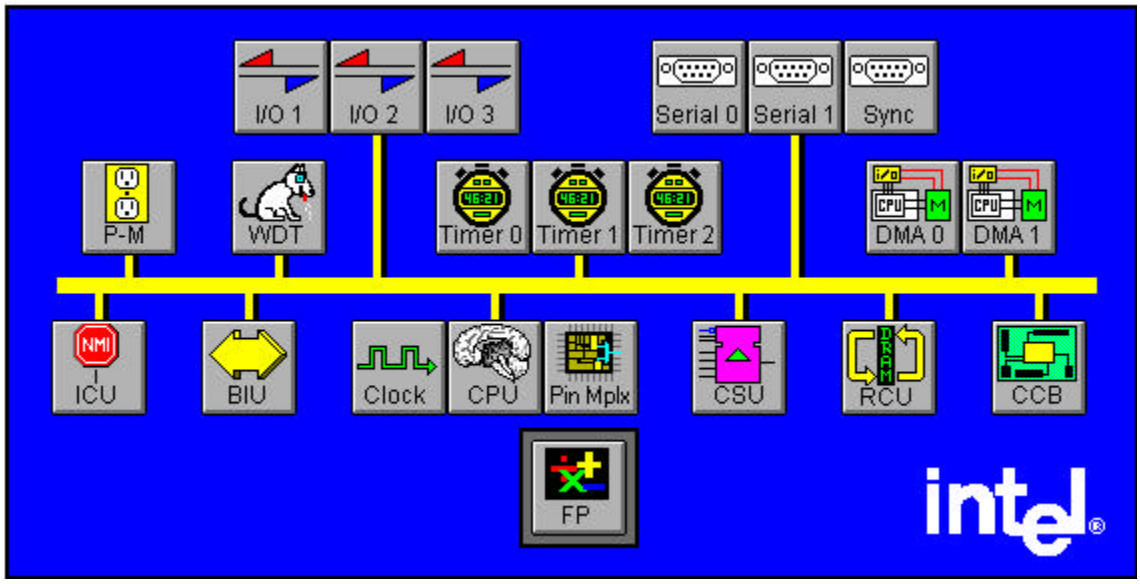

Figure 3-1: Intel386™ Organization

Figure 3-1 represents a simplified view of Intel386™EX Embedded Processor. The Power Management Unit (P-M) allows processor to go into Idle mode or Powerdown Mode. Idle mode allows to freeze the CPU clock, but leave peripherals functioning, therefore, reducing current consumption. This mode exited via NMI, SMI, or unmasked interrupt. Powerdown mode allows to freeze all clocks and reduce current consumption to leakage (uA). This mode exited by NMI, SMI, or unmaskable interrupt.

The Programmable Interrupt Control Unit (ICU) has two 8259A modules connected in master/slave configuration. The interrupt structure is compatible with PC/DOS architecture. It supports eight external maskable interrupt inputs, 36 external interrupts with cascaded 82C59s, and seven internal peripheral sources.

Bus Interface Unit (BIU) allows to access up to 64Mbyte memory address range, and 64Kbyte I/O address range. In addition it allows to do 8 and 16-bit dynamic bus sizing, and has separate RD# and WR# signals for glue-less SRAM_EPROM interface.

Watchdog Timer Unit (WDT) allows recovery from system failures caused by runaway software. It is also a usable 32-bit general-purpose timer. WDT's bus monitor function allows recovery from "ready hang" situations.

The processor has three flexible I/O ports, which are individually configurable as input, output, or bidirectional open drain. Ports 1 and 2 have 8mA drive capability,

port 3 has 16mA drive capability.

The CPU clock will give frequency from 0 to 16 MHz when operating voltage is 3.3V. The clock has 50% duty cycle. In addition, it has a programmable divider for timers and synchronous communications.

Three independent 16-bit timers constitute the Timer Control Unit. Each timer can operate in 1 of 6 modes:

(a) Interrupt on terminal count;
(b) Hardware retriggerable one-shot;
(c) Rate generator;
(d) Square wave mode;
(e) Software triggered mode, and
(f) Hardware triggered mode (retriggerable)

Each of these timers can serve as an internal or external clocking source.

Chip Select Unit (CSU) has eight programmable memory and peripheral chip selects, supports SMM memory addressing and enhances READY generation logic. CSU has programmable wait states (0 – 31) and allows overlapping of chip selects.

Refresh Control Unit (RCU) provides periodic DRAM refresh cycles. It supports DRAM and PSRAM. The refresh interval and address range are programmable.

Chip Configuration Block (CCB) has two sets of registers: pin configuration registers and chip configuration registers. The pin configuration registers determine pin functions, the chip configuration registers allow versatile module inter-connection. CCB allows to configure processor for one of four operation modes:

(a) DOS compatible;
(b) Non-Intrusive DOS compatible;
(c) Enhanced DOS;
(d) Non-DOS.

The processor has a Direct Memory Access Unit (DMA), which consists of two independent DMA channels. Through these channels, the processor can transfer data between memory and I/O in any combination. Each DMA channel transfers using 8 or 16-bit width, supports fly-by transfers. A transfer can be requested internally (timers and SCU), or through software. DMA channels support full 26-bit source and destination pointers and 26-bit transfer count allowing 16Mbyte block transfers.

For serial communications, the processor has one synchronous and two asynchronous serial ports. The 16-bit synchronous serial port allows full duplex synchronous communications. It has independent transmitter and receiver, capable of operating at different baud rates. Achievable transfer rates exceed 6Mbaud. Two independent asynchronous serial channels have integral programmable baud-rate generator (DC to 512Kbaud). In addition, they have modem control functions, double-buffered transmit/receive, and fully programmable serial interface characteristics. Error detection functions include false start bit detection.

4. Lists

1.1 Embedded Intel386™ Family Processors: Side by Side Comparison

Table 4-1: Speed/Voltage Comparison

Processor Type	Speed	Voltage
Intel386™ SXSA	25 MHz	5 V
	33 MHz	5 V
	40 MHz	5 V
Intel386™ CXSA	25 MHz	5 V
	33 MHz	5 V
	40 MHz	5 V
Intel386™ CXSB	16 MHz	2.7 – 3.3 V
	25 MHz	3.0 – 3.6 V
Intel 386™ EX	16 MHz	2.7 – 3.3 V
	20 MHz	3.0 – 3.6 V
	25 MHz	4.5 – 5.5 V

Table 4-2: I/O Structure Comparison

Processor Type	Input Levels	I/O Pins
Intel386™ SXSA	TTL	0
Intel386™ CXSA	TTL	0
Intel386™ CXSB	CMOS	0
Intel 386™ EX	CMOS	24

Table 4-3: Power Options

Processor Type	Idle	Powedown
Intel386™ SXSA	No	No
Intel386™ CXSA	No	No
Intel386™ CXSB	No	No
Intel 386™ EX	Yes	Yes

Table 4-4: Peripheral Comparison

	Intel386™ SXSA	Intel386™ CXSA	Intel386™ CXSB	Intel 386™ EX
Chip Select Ready Logic	186 Style	186 Style	186 Style	186 Style
Chip Select Pins	None	None	None	None
Clock Generation Unit	Yes	Yes	Yes	Yes
DMA Channels	None	None	None	2

	Intel386™ SXSA	Intel386™ CXSA	Intel386™ CXSB	Intel 386™ EX
Direct Numeric Interface	Yes (Intel387™)	Yes (Intel387™)	Yes (Intel387™)	Yes (Intel387™)
Interrupt Control Unit	No	No	No	Yes
Refresh Control Unit	No	No	No	Yes
SIO	None	None	None	2
SSIO	None	None	None	1
Timer/Counter	None	None	None	3
WDT	No	No	No	Yes

Table 4-5: Package Offerings

Processor Type	100-Pin PQFP	100-Pin DQFP	132-Pin PQFP	144-Pin TQFP
Intel386™ SXSA	Yes	Yes	No	No
Intel386™ CXSA	Yes	Yes	No	No
Intel386™ CXSB	Yes	Yes	No	No
Intel 386™ EX	No	No	Yes	Yes

5. Interface Requirements and Specifications

The DCH Flight Hardware will be interfaced to science systems and communication systems via RS232 serial connection. If there will be too much noise, RS432 serial connection will be used instead. Interfacing of the Flight Hardware with other systems will depend on their requirements. The sensors and systems that will require periodic checks of their status might be memory-mapped. Sensors and systems that will send a signal to CPU if some parameters are out of determined range will generate an interrupt. One sensor or system might be memory-mapped and, in addition, generate an interrupt.

6. Current Status

Currently, we are in stage of determining more detailed requirements for DCH Flight Hardware and gathering more information about Intel386™EX Embedded Processor architecture, 386EX based design, and spacecraft hardware design.

7. Test Plan

All Flight Hardware will be designed modularly, from bottom-up, meaning that first, the small modules will be designed and tested separately. Then they will be connected one by one together with tests after every connection. For example, first,

the CPU section with clock and reset/powerup circuitry will be designed, assembled and tested with the CPU running in free-run. Then, the memory section will be connected and tested with the CPU section. Next, I/O ports, serial ports, interrupt circuitry etc. More detailed test plan will be developed after developing and analyzing the requirements set for the DCH Flight Hardware.

8. Concerns and Open Issues

8.1 CPU and Components radiation hardness

Since Intel does not test its products on radiation hardness, the exact amount of radiation that Intel386™EX can withstand is mostly a guess. I have contacted Intel regarding a location of 3rd party testing house to get the needed information. The same concern applies to other components we might be using in our design.

8.2 System requirements and interface requirements

This is still an open issue. More detailed set of requirements has to be determined and analyzed. In order to do this, more information is needed about conditions of space flight. In particular, we need information about possible vibrations and overloads that might occur during space shuttle launch. In addition, we need information about possible temperatures during the space shuttle launch and after the satellite is in orbit.

We need to figure out the space requirements for our hardware. We need to know how many cubic centimeters of space do we have available for all our hardware, what shape the PC boards will have to be, and what kind of mounting options will we to mount our PC boards on the satellite.

We need more detailed information from other teams about how our system will have to communicate with their systems, what control functions our system will have to provide to systems, how many sensors are they planning to have, and what kind of sensors are those going to be. We have to know if our system will have to monitor their sensors and systems periodically or just wait for their signal. If periodically, then what would be the length of the period? If wait for the signal from other system/sensor, then priorities will have to be set for this kind of signals.

9. References

[1] Intel386™EX data sheet; Document 27242006.pdf obtained at Intel Literature Center, http://developer.intel.com/design/litcentr/index.htm

[2] Intel386™EX User's Manual; Document 27248502.pdf obtained at Intel Literature Center, http://developer.intel.com/design/litcentr/index.htm

[3] 80386 Technical Reference; Strauss, Edmund. A Brady Book New York: New York, 1987

[4] Intel ApBUILDER, version 2.21, Fact Sheets.